CLAIMS

1. A method for providing immediate virtual memory within a computer system, the method comprising:

allocating a new translation for a virtual memory page; and

setting one or more bit flags within the translation to indicate that the translation specifies an immediate virtual memory page.

2. The method of claim 1 wherein the new translation is a translation look-aside buffer entry allocated within a translation look-aside buffer.

3. The method of claim 2 wherein the new translation look-aside buffer entry is a translation look-aside buffer entry allocated within a virtual hash page table.

4. The method of claim 1 wherein the new translation is allocated within a memory-resident operating-system data structure.

5. The method of claim 1 wherein, when immediate virtual memory is accessed by a READ access instruction, a specified value is returned.

6. The method of claim 5 wherein the specified value is generated by a processor logic circuit.

7. The method of claim 5 wherein the specified value is obtained from a default-valued processor register.

8. The method of claim 5 wherein the specified value is specified by one of:

a software specification within an operating system; or

a hardware logic circuit.

9. The method of claim 5 wherein the specified value is 0.

10. The method of claim 5 wherein the specified value is any fixed, non-zero bit pattern of any size.

11. The method of claim 5 wherein the specified value is a random number obtained by processor logic algorithmically, from electronic noise, or from another physical source.

12. The method of claim 1 wherein, when immediate virtual memory is accessed by a WRITE access instruction, an exception is generated to allow an operating system to allocate and initialize a physical memory page corresponding to the virtual memory page.

13. A computer processor that provides architecture support for immediate virtual memory, the computer processor comprising:

processor logic for executing computer instructions and fetching instructions and data from memory; and

processor logic for reading one or more control bits within a translation and determining whether or not a corresponding unit of memory is immediate.

14. The computer processor of claim 13 further including:

processor logic that, upon READ access to memory determined to be immediate, returns a specified value; and

processor logic that, upon WRITE access to immediate memory, generates an immediate memory exception to allow an operating system to allocate and initialize physical memory corresponding to the immediate memory.

15. The computer processor of claim 14 wherein the specified value is generated by a processor logic circuit.

16. The computer processor of claim 14 wherein the specified value is obtained from a specified processor register.

17. The computer processor of claim 14 wherein the specified value is 0.

18. The computer processor of claim 14 wherein the specified value is any fixed, non-zero bit pattern of any size.

19. The computer processor of claim 14 wherein the specified value is a random number obtained by processor logic algorithmically, from electronic noise, or from another physical source.

20. The computer processor of claim 14 wherein the specified value is specified by one of:

a software specification within an operating system; or

a hardware logic circuit.

21. An operating system that allocates an immediate virtual memory page within a computer system by:

allocating a new translation for the virtual memory page; and

setting an immediate bit flag within the translation to indicate that the corresponding virtual memory page is immediate, with no allocated physical memory.

22. The operating system of claim 21 wherein the new translation is a translation look-aside buffer entry allocated within a translation look-aside buffer.

23. The operating system of claim 22 wherein the new translation look-aside buffer entry is a translation look-aside buffer entry allocated within a virtual hash page table.

24. The operating system of claim 21 wherein the new translation is allocated within a memory-resident operating-system data structure.

25. The operating system of claim 21 wherein, when an immediate virtual memory page is accessed by a READ access instruction, a specified value is returned.

26. The operating system of claim 25 wherein the specified value is generated by a processor logic circuit.

27. The operating system of claim 25 wherein the specified value is obtained from a specified processor register.

28. The operating system of claim 25 wherein the specified value is 0.

29. The operating system of claim 25 wherein the specified value is -1 in two's complement arithmetic.

30. The operating system of claim 25 wherein the specified value is a random number obtained by processor logic algorithmically, from electronic noise, or from another physical source.

31. The operating system of claim 21 wherein, when an immediate virtual memory page is accessed by a WRITE access instruction, an immediate-virtual-memory-page exception is generated to allow the operating system to allocate and initialize a physical memory page corresponding to the virtual memory page.